

Laboratory 1

(Due date : **002/003**: January 28th, **004**: January 22nd, **005**: January 23rd)

OBJECTIVES

- ✓ Introduce VHDL Coding for FPGAs.
- ✓ Learn to write testbenches in VHDL.
- ✓ Learn the Xilinx FPGA Design Flow with the Vivado HL: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream on the Nexys™ A7-50T Board.

VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

NEXYS™ A7-50T FPGA TRAINER BOARD SETUP

- The Nexys A7-50T Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- Nexys A7-50T documentation: Available in [class website](#).

FIRST ACTIVITY (100/100)

- **PROBLEM** (Majority function): An LED is lit ($f=1$) if any three or all four of the switches (variables a, b, c, d) are equal, where '1' represents the ON position of a switch and '0' the OFF position.
For example: if $abcd = 1010 \rightarrow f = 0$. If $abcd=0010 \rightarrow f = 1$.

- ✓ Complete the truth table for this circuit:

- ✓ Derive (simplify if possible) the Boolean expression:

$f =$

a	b	c	d	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

- **VIVADO DESIGN FLOW FOR FPGAs – NEXYS A7-50T (follow this order strictly):**
 - ✓ Create a new Vivado Project. Select the **XC7A50T-1CSG324 Artix-7 FPGA** device.
 - ✓ Write the VHDL code that implements the simplified Boolean expression. Synthesize your circuit (Run Synthesis).
 - ✓ Write the VHDL testbench to test every possible combination of the inputs.
 - ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**
 - ✓ I/O Assignment: Create the XDC file.
Nexys A7-50T Board: Use **SW0**, **SW1**, **SW2**, **SW3** as inputs, and **LED0** as the output. All I/Os are active high.
 - ✓ Implement your design (Run Implementation).
 - ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
 - ✓ Generate the bitstream file (Generate Bitstream).
 - ✓ Download the bitstream on the FPGA (Open Hardware Manager) and test. **Demonstrate this to your TA.**
- Submit (as a .zip file) the generated files: VHDL code, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____

Date: _____